Remarks

Claims 47-67 are pending in this application. Claims 47-63 are withdrawn from consideration. Claims 64-67now stand rejected.

Claims 1-46 have been cancelled.

Claim Rejections - 35 U.S.C. § 112

Claims 66 and 67 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

Claims 66 and 67 have been amended to add a limitation that "the low stress LPPECVD-LTO layer and the high stress LPPECVD-LTO layer have densified to form a single LTO layer." Support for these amendments is found in the Specification at page 9, ll. 14-16.

Accordingly, claims 66 and 67 are now allowable under 35 U.S.C. § 112, first paragraph.

Claim Rejections - 35 U.S.C. § 102

Claim 64 is rejected under 35 U.S.C. § 102(b) as anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as obvious over Barth et al. (US 2002/0076917)

Applicants respectfully traverse the present rejection for the following reasons. Independent claim 64 is directed to a wafer having a two layer backside seal. The components of clim 64 are summarized as follows:

a) a wafer substrate (. . .) and

b) a two layer backside seal comprising

b1) a low stress LPPECVD-LTO layer adjacent to the wafer substrate

b2) a high stress LPPECVD-LTO layer adjacent to b1)

b3) the stress in b1) is less than 100 MPa and

b4) the stress in b2) is less than 300 MPa and

b5) the stress in b2) is higher than in b1).

The claimed wafer has the property to reducing autodoping, i.e., the diffusion of gaseous dopants from the backside of the substrate to the front side, and to provide significantly greater suppression of visual edge epi-haze (Specification, p. 1, l. 14 and p. 7, l. 7-9).

Barth et al. is directed to a metallization insulating structure used in semiconductor devices. The insulating structure is capable to prevent degradation in semiconductor device wiring. In the context of Barth et al., degradation encompasses "corrosion" or "poisoning" of metal and the negative effect on the reliability or electrical properties of the interconnection (Barth et al., para. [0019]).

Therefore, Barth et al. clearly does not disclose a layer structure which is a backside seal of a wafer substrate as required by independent claim 1. The layers set forth in Barth et al. are not suitable to seal the backside of a wafer. In particular, Barth et al. does not include a two layer backside seal.

According to Barth et. al, paragraph [0023], the structure is a two component dual damascene dielectric for copper wiring consisting of low stress SiO_2 (USG) and low stress SiO_xF_y (FSG):

> This invention relates to a structure with a two component dual damascene dielectric for copper wiring **consisting of low stress SiO_2 (USG), and low stress SiO_xF_y (FSG)**. In this structure, the lower and middle portions of the vias are surrounded by USG; the upper portion of the vias are surrounded by either FSG or USG; and the wiring trenches are surrounded by an

> FSG insulator. Note the interface between the USG and FSG insulators need not correspond with the intersection of the vias and lines, but could be tailored for optimal performance, manufacturability and reliability. Typically the overall height of the FSG insulator would be greater than the height of the interconnection lines, while still maintaining a fraction of the via height surrounded by USG. Finally note that a layer of silicon nitride or other etch stops could be included between the USG and FSG dielectrics or at the bottom of the wire trench, to allow for a selective trench RIE process and more controlled trench depth.
>
> Barth et al., para. [0023]

Significantly, both the first and second layers in Barth et al. are low stress layers. Claim 64 requires a low stress LPPECVD-LTO low temperature oxide layer adjacent to the wafer substrate and a high stress LPPECVD-LTO layer adjacent a low stress LPPECVD-LTO low temperature oxide layer. Each of these refers to low temperature oxide layers. Barth et. al. does not disclose an adjacent low stress LPPECVD-LTO layer and a high stress LPPECVD-LTO layer with the stress high stress LPPECVD-LTO layer being higher than the stress in the low stress LPPECVD-LTO layer.

In should also be appreciated that the second layer (the FSG layer) in Barth et al. is not a mere oxide layer, but a doped oxide layer. (Barth et al., para. [0024]). Such dopants are usually substances such as fluoride which causes capacitance/stress tradeoffs. This is further evidence that a high stress LPPECVD-LTO layer is not a component in the Barth et al. disclosure.

Accordingly, for at least these reasons, claim 64 is allowable under 35 U.S.C. § 102(b) or, in the alternative, under 35 U.S.C. § 103(a) over Barth et al.

Claim Rejections – 35 U.S.C. § 103

Claim 65 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Barth et al. (US 2002/0076917) as applied to claim 64 above, in view of Chen (US 6,440,840).

Claim 65 depends from claim 64 which is shown above to be allowable. Accordingly, claim 65 is now allowable under 35 U.S.C. § 103(a) over Barth et al. as applied to claim 64 above, in view of Chen.

Conclusion

Applicants have made a genuine effort to respond to each of the Examiner's objections and rejections in advancing the prosecution of this case. Applicants believe that all formal and substantive requirements for patentability have been met and that this case is in condition for allowance, which action is respectfully requested. If any additional issues need to be resolved, the Examiner is invited to contact the undersigned at his earliest convenience.

Please charge any fees or credit any overpayments as a result of the filing of this paper to our Deposit Account No. 02-3978.

Respectfully submitted,

JIN-XING LI ET AL.

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